1

GaN Technology Overview

1.1 Silicon Power Metal Oxide Silicon Field Effect Transistors 1976–2010

For over four decades, power management efficiency and cost have improved steadily as innovations in power metal oxide silicon field effect transistor (MOSFET) structures, technology, and circuit topologies have kept pace with the growing need for electrical power in our daily lives. In the new millennium, however, the rate of improvement has slowed as the silicon power MOSFET asymptotically approaches its theoretical bounds.

Power MOSFETs first appeared in 1976 as alternatives to bipolar transistors. These majority-carrier devices were faster, more rugged, and had higher current gain than their minority-carrier counterparts (for a discussion of basic semiconductor physics, a good reference is [1]). As a result, switching power conversion became a commercial reality. Among the earliest high-volume consumers of power MOSFETs were AC–DC switching power supplies for early desktop computers, followed by variable-speed motor drives, fluorescent lights, DC–DC converters, and thousands of other applications that populate our daily lives.

One of the first power MOSFETs was the IRF100 from International Rectifier Corporation, introduced in November 1978. It boasted a 100 V drain-source breakdown voltage and a 0.1 Ω on-resistance ($R_{DS(on)}$), the benchmark of the era. With a die size over 40 mm^2 and with a $34 price tag, this product was not destined to supplant the venerable bipolar transistor immediately. Since then, several manufacturers have developed many generations of power MOSFETs. Benchmarks have been set, and subsequently surpassed, each year for 40-plus years. As of the date of this writing, the 100 V benchmark arguably is held by Infineon with the BSZ096N10LS5. In comparison with the IRF100 MOSFET's resistivity figure of merit (4 Ω mm^2), the BSZ096N10LS5 has a figure of merit of 0.060 Ω mm^2. That is almost at the theoretical limit for a silicon device [2].

There are still improvements to be made in power MOSFETs. For example, superjunction devices and IGBTs have achieved conductivity improvements beyond the theoretical limits of a simple vertical, majority-carrier MOSFET. These innovations may still continue for quite some time and certainly will be able to leverage the low-cost structure of the power MOSFET and the know-how of a well-educated base of designers who, after many years, have learned to squeeze every ounce of performance out of their power conversion circuits and systems.

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1.2 The Gallium Nitride Journey Begins

Gallium nitride (GaN) is called a wide bandgap (WBG) semiconductor due to the relatively large bonding energy of the atomic components in its crystal structure (silicon carbide [SiC] is the other most common WBG semiconductor). GaN HEMT (High Electron Mobility Transistors) devices first appeared in about 2004 with depletion-mode radio frequency (RF) transistors made by Eudyna Corporation in Japan. Using GaN-on-SiC substrates, Eudyna successfully produced transistors designed for the RF market [3]. The HEMT structure was based on the phenomenon first described in 1975 by Mimura et al. [4] and in 1994 by Khan et al. [5], which demonstrated the unusually high electron mobility described as a two-dimensional electron gas (2DEG) near the interface between an AlGaN and GaN heterostructure interface. Adapting this phenomenon to GaN grown on SiC, Eudyna was able to produce benchmark power gain in the multigigahertz frequency range. In 2005, Nitronex Corporation introduced the first depletion-mode RF HEMT device made with GaN grown on silicon wafers using their SIGANTIC® technology.

GaN RF transistors have continued to make inroads in RF applications as several other companies have entered the market. Acceptance outside of this application, however, has been limited by device cost as well as the inconvenience of depletion-mode operation (normally conducting and requires a negative voltage on the gate to turn the device off).

In June 2009, Efficient Power Conversion Corporation (EPC) introduced the first enhancement-mode GaN on silicon (eGaN®) field effect transistors (FETs) designed specifically as power MOSFET replacements (since eGaN FETs do not require a negative voltage to be turned off). At the outset, these products were produced in high volume at low cost by using standard silicon manufacturing technology and facilities. Since then, Matsushita, Transphorm, GaN Systems, ON Semiconductor, Panasonic, TSMC, Navitas, and Infineon, among others, have announced their intention to manufacture GaN transistors for the power conversion market.

The basic requirements for semiconductors used in power conversion are efficiency, reliability, controllability, and cost effectiveness. Without these attributes, a new device structure would not be economically viable. There have been many new structures and materials considered as a successor to silicon; some have been economic successes, others have seen limited or niche acceptance. In the next section, we will look at the comparison between silicon, SiC, and GaN as platform candidates to dominate the next-generation of power transistors.

1.3 GaN and SiC Compared with Silicon

Silicon has been a dominant material for power management since the late 1950s. The advantages silicon had over earlier semiconductors, such as germanium or selenium, could be expressed in four key categories:

- Silicon enabled new applications not possible with earlier materials.
- Silicon proved more reliable.
- Silicon was easier to use in many ways.
- Silicon devices cost less.

Table 1.1 Material properties of GaN, 4H-SiC, and Si.

Parameters		Silicon	GaN	SiC
Band Gap E_g	eV	1.12	3.39	3.26
Critical Field E_{crit}	MV/cm	0.23	3.3	2.2
Electron Mobility μ_n	$cm^2/V \cdot s$	1400	1500	950
Permittivity ε_r		11.8	9	9.7
Thermal Conductivity λ	W/cm•K	1.5	1.3	3.8

All of these advantages stemmed from the basic physical properties of silicon combined with a huge investment in manufacturing infrastructure and engineering. Let us look at some of those basic properties and compare them with other successor candidates. Table 1.1 identifies five key electrical properties of three semiconductor materials contending for the power management market.

One way of translating these basic crystal parameters into a comparison of device performance is to calculate the best theoretical performance achievable for each of the three candidates. For power devices, there are many characteristics that matter in the variety of power conversion systems available today. Five of the most important are: conduction efficiency (on-resistance), breakdown voltage, size, switching efficiency, and cost.

In the next section, the first four of the material characteristics in Table 1.1 will be reviewed, leading to the conclusion that both SiC [6] and GaN are capable of producing devices with superior on-resistance, breakdown voltage, and a smaller-sized transistor compared to Si. In Chapter 2, how these material characteristics translate into superior switching efficiency for a GaN transistor will be explored and in Chapter 17, how a GaN transistor can also be produced at a lower cost than a silicon MOSFET of equivalent performance will be addressed.

1.3.1 Bandgap (E_g)

The bandgap of a semiconductor is related to the strength of the chemical bonds between the atoms in the lattice. These stronger bonds mean that it is harder for an electron to jump from one site to the next. Among the many consequences are lower intrinsic leakage currents and higher operating temperatures for higher bandgap semiconductors. Based on the data in Table 1.1, GaN and SiC both have higher bandgaps than silicon.

1.3.2 Critical Field (E_{crit})

The stronger chemical bonds that cause the wider bandgap also result in a higher critical electric field needed to initiate impact ionization, which results in avalanche breakdown. The voltage at which a device breaks down can be approximated with the formula:

$$V_{BR} = \tfrac{1}{2} w_{drift} \cdot E_{crit} \tag{1.1}$$

The breakdown voltage of a device (V_{BR}) is therefore proportional to the width of the drift region (w_{drift}). In the case of SiC and GaN, the drift region can be 10 times smaller than in silicon for the same breakdown voltage. In order to support this electric field, there need to be carriers in the drift region that are depleted away at the point where the device reaches the critical field. This is where there is a huge gain in devices with high critical fields. The number of electrons (assuming an N-type semiconductor) between two terminals can be calculated using Poisson's equation:

$$q \cdot N_D = \varepsilon_o \cdot \varepsilon_r \cdot E_{crit} / w_{drift} \tag{1.2}$$

In this equation q is the charge of the electron ($1.6 \cdot 10^{-19}$ C), N_D is the total number of electrons in the volume, ε_o is the permittivity of a vacuum measured in Farads per meter ($8.854 \cdot 10^{-12}$ F/m), and ε_r is the relative permittivity of the crystal compared to a vacuum. In its simplest form under DC conditions, permittivity is the dielectric constant of the crystal.

Referring to Eq. (1.2), it can be seen that if the critical field of the crystal is 10 times higher, from Eq. (1.1), the electrical terminals can be 10 times closer together. Therefore, the number of electrons, N_D, in the drift region can be 100 times greater, but only have one-tenth the distance to travel. This is the basis for the ability of GaN and SiC to outperform silicon in power conversion.

1.3.3 On-Resistance ($R_{DS(on)}$)

The theoretical on-resistance of a one square millimeter majority-carrier device (measured in ohms [$\Omega \cdot mm^2$]) is therefore

$$R_{DS(on)} = w_{drift} / q \cdot \mu_n \cdot N_D \tag{1.3}$$

where μ_n is the mobility of electrons. Combining Eqs. (1.1) to (1.3) produces the following relationship between breakdown voltage and on-resistance:

$$R_{DS(on)} = 4 \cdot V^2_{BR} / \varepsilon_o \cdot \varepsilon_r \cdot \mu_r \cdot E^3_{crit} \tag{1.4}$$

This equation can now be plotted as shown in Figure 1.1 for Si, SiC, and GaN. This plot is for an ideal structure. Real semiconductors are not always ideal structures and, therefore, it is always a challenge to achieve the theoretical limit. In the case of silicon MOSFETs, it took 30 years.

1.3.4 The Two-Dimensional Electron Gas (2DEG)

The natural structure of crystalline GaN, a hexagonal structure named "wurtzite," is shown in Figure 1.2a and the 4H-SiC structure is shown in Figure 1.2b. Because both structures are very chemically stable, they are mechanically robust and can withstand high temperatures without decomposition. The wurtzite crystal structure gives GaN piezoelectric properties that lead to its ability to achieve very high conductivity compared with either silicon or SiC.

Piezoelectricity in GaN is predominantly caused by the displacement of charged elements in the crystal lattice. If the lattice is subjected to strain, the deformation will cause a miniscule shift in the atoms in the lattice that generate an electric field – the

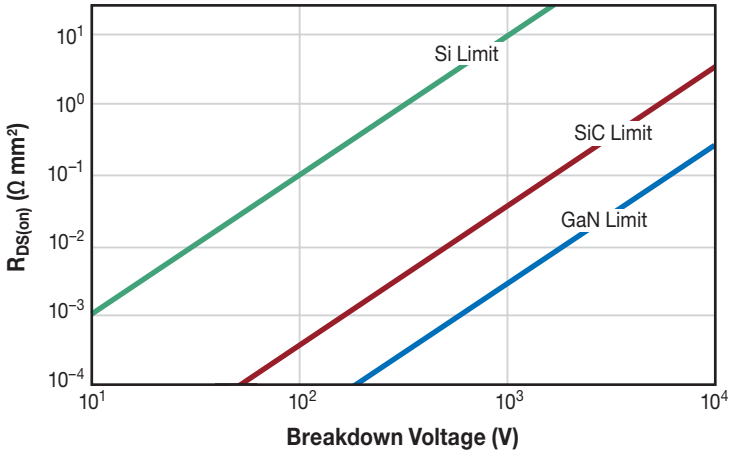

Figure 1.1 Theoretical on-resistance for a one square millimeter device versus blocking voltage capability for Si, SiC, and GaN based power devices.

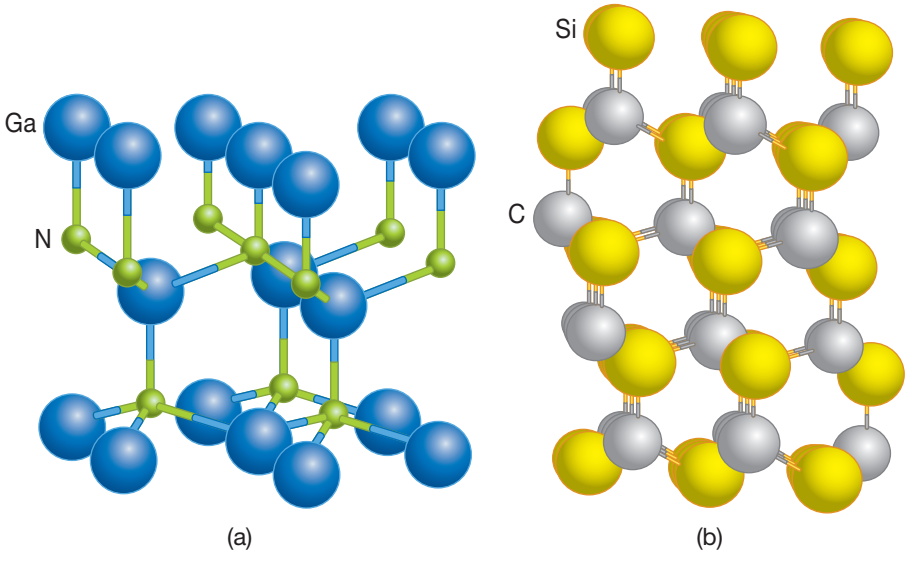

Figure 1.2 (a) Schematic of wurtzite GaN. (b) Schematic of 4H-SiC.

higher the strain, the greater the electric field. By growing a thin layer of AlGaN on top of a GaN crystal, a strain is created at the interface that induces a compensating 2DEG, as shown schematically in Figure 1.3 [7–9]. This 2DEG is used to efficiently conduct electrons when an electric field is applied across, as shown in Figure 1.4.

This 2DEG is highly conductive, in part due to the confinement of the electrons to a very small region at the interface. This confinement increases the mobility of electrons from about 1000 $cm^2/V{\cdot}s$ in unstrained GaN to between 1500 and 2000 cm^2/V s in the 2DEG region. The high concentration of electrons with very high mobility is the basis for the HEMT, the primary subject of this book.

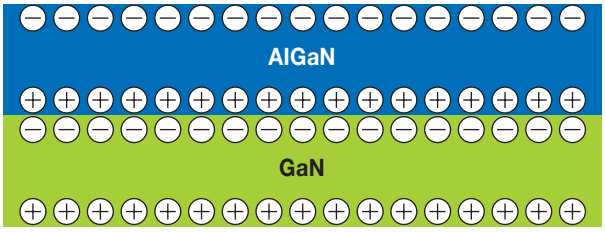

Figure 1.3 Simplified cross section of a GaN/AlGaN heterostructure showing the formation of a 2DEG due to the strain-induced polarization at the interface between the two materials.

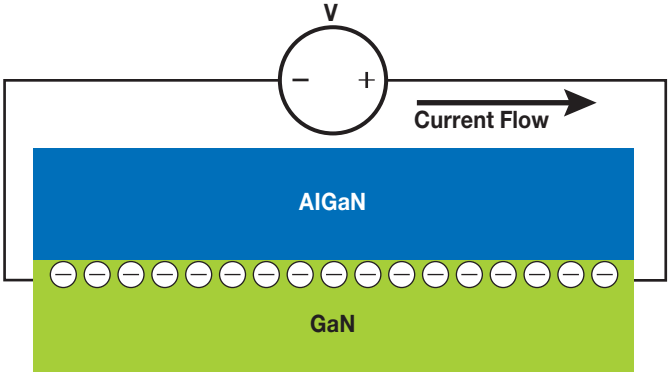

Figure 1.4 By applying a voltage to the 2DEG an electric current is induced in the crystal.

1.4 The Basic GaN Transistor Structure

The basic depletion-mode GaN transistor structure is shown in Figure 1.5. As with any power FET, there are gate, source, and drain electrodes. The source and drain electrodes pierce through the top AlGaN layer to form an ohmic contact with the underlying 2DEG. This creates a short circuit between the source and the drain unless the 2DEG "pool" of electrons is depleted and the semi-insulating GaN crystal can block the flow of current. In order to deplete the 2DEG, a gate electrode is placed on top of the AlGaN layer. When a negative voltage relative to both drain and source electrodes is applied to the gate, the electrons in the 2DEG are depleted out of the device. This type of transistor is called a depletion-mode, or d-mode, HEMT.

There are two common ways to produce a d-mode HEMT device. The initial transistors introduced in 2004 had a Schottky gate electrode that was created by depositing a metal layer directly on top of the AlGaN. The Schottky barrier was formed using metals such as Ni–Au or Pt [10–12]. Depletion-mode devices have also been made using an insulating layer and metal gate similar to a MOSFET [13]. Both types are shown in Figure 1.6.

In power conversion applications, d-mode devices are inconvenient because, at the startup of a power converter, a negative bias must first be applied to the power devices. If this negative bias is not applied first, a short circuit will result, leading to catastrophic failure. An enhancement-mode (e-mode) device, on the other hand, would not suffer this limitation. With zero bias on the gate, an e-mode device is OFF

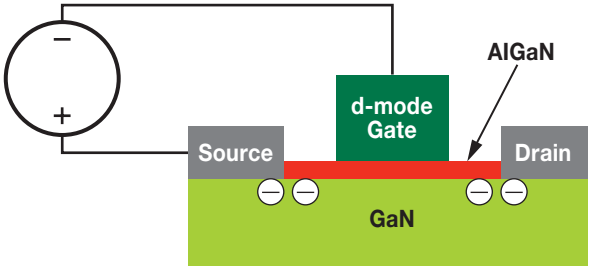

Figure 1.5 By applying a negative voltage to the gate of the device, the electrons in the 2DEG are depleted out of the device. This type of device is called a depletion-mode (d-mode) HEMT.

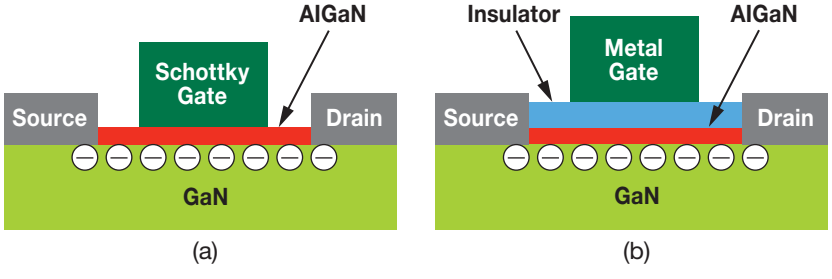

Figure 1.6 Cross section of a basic depletion-mode GaN HEMT with (a) Schottky gate or (b) insulating gate.

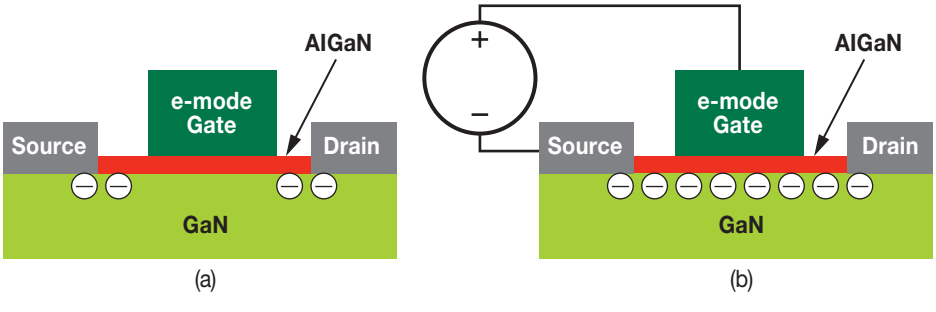

Figure 1.7 (a) An enhancement-mode (e-mode) device depletes the 2DEG with zero volts on the gate. (b) By applying a positive voltage to the gate, the electrons are attracted to the surface, re-establishing the 2DEG.

(Figure 1.7a) and will not conduct current until a positive voltage is applied to the gate, as illustrated in Figure 1.7b.

There are five popular structures that have been used to create enhancement-mode devices: recessed gate, implanted gate, pGaN gate, direct drive hybrid, and cascode hybrid.

1.4.1 Recessed Gate Enhancement-Mode Structure

The recessed gate structure has been discussed extensively in the literature [14] and is created by thinning the AlGaN barrier layer above the 2DEG (see Figure 1.8). By making the AlGaN barrier thinner, the amount of voltage generated by the piezoelectric field is

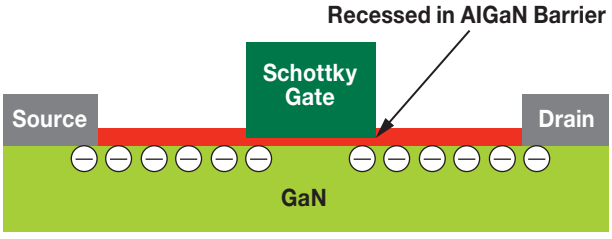

Figure 1.8 By etching away part of the AlGaN barrier layer a recessed gate e-mode transistor can be fabricated.

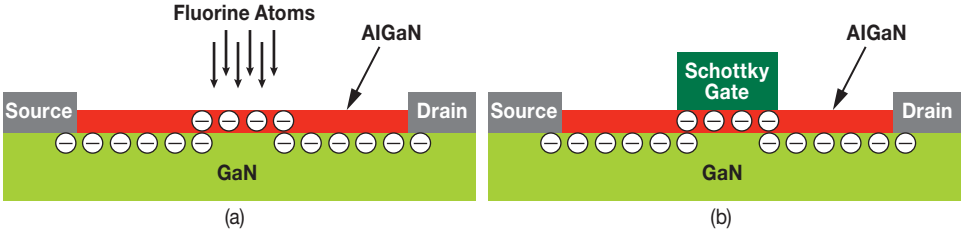

Figure 1.9 (a) By implanting fluorine atoms into the AlGaN barrier layer negative charges are trapped in the barrier. (b) A Schottky gate now can be used to reconstruct the 2DEG when a positive voltage is applied.

reduced proportionally. When the voltage generated is less than the built-in voltage of the Schottky gate metal, the 2DEG is eliminated with zero bias on the gate. With positive bias, electrons are attracted to the AlGaN interface and complete the circuit between the source and drain.

1.4.2 Implanted Gate Enhancement-Mode Structure

Shown in Figure 1.9a and b is a method for creating an enhancement-mode device by implanting fluorine atoms into the AlGaN barrier layer [15]. These fluorine atoms create a "trapped" negative charge in the AlGaN layer that depletes the 2DEG underneath. By adding a Schottky gate on top, an enhancement-mode HEMT is created.

1.4.3 pGaN Gate Enhancement-Mode Structure

The first enhancement-mode devices sold commercially had a positively charged (p-type) GaN layer grown on top of the AlGaN barrier (see Figure 1.10) [16]. The positive charges in this pGaN layer have a built-in voltage that is larger than the voltage generated by the piezoelectric effect, thus depleting the electrons in the 2DEG and creating an enhancement-mode structure [17].

1.4.4 Hybrid Normally Off Structures

An alternative to building a single-chip enhancement-mode GaN transistor is to place an enhancement-mode silicon MOSFET in series with a depletion-mode HEMT device [18, 19]. Figure 1.11 shows two variations of these hybrid normally off structures.

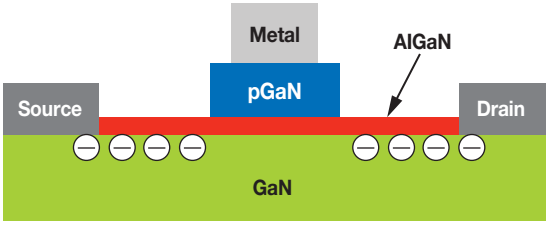

Figure 1.10 By growing a p-type GaN layer on top of the AlGaN, the 2DEG is depleted at zero volts on the gate.

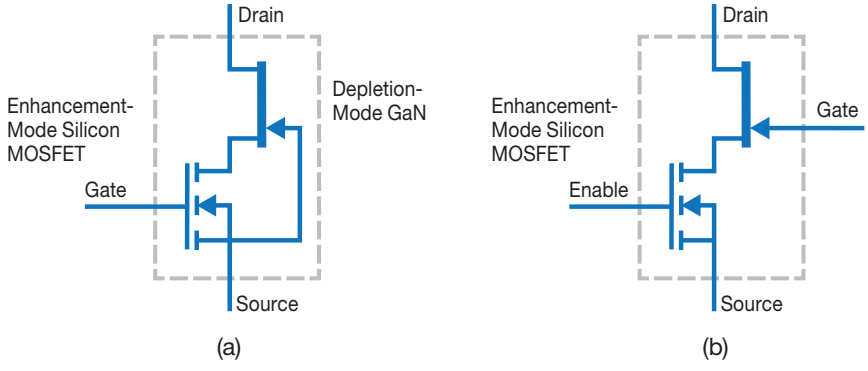

Figure 1.11 Schematic of low-voltage enhancement-mode silicon MOSFET in series with a depletion-mode GaN HEMT. (a) Cascode circuit and (b) enable/direct-drive circuit.

In the cascode circuit, shown in Figure 1.11a, the gate of the depletion-mode GaN HEMT is connected to the source of the enhancement-mode Si MOSFET. When the MOSFET is turned on with a positive voltage on the gate, the depletion-mode GaN transistor's gate voltage goes to near-zero volts and turns on as a result. Current can now pass through the depletion-mode GaN HEMT and the MOSFET, which is connected in series with the GaN HEMT. When the voltage on the MOS gate is removed, a negative voltage is created between the depletion-mode GaN transistor gate and its source electrode, turning the GaN device off.

The second variation of this circuit has been described as an "enable circuit" or "direct drive circuit," shown in Figure 1.11 [20]. Here, the gate of the depletion-mode GaN HEMT is directly accessible to the external gate driver. The circuit has four terminals: gate, drain, source, and enable. Compared with the cascode configuration, this variation has the advantage of more direct control over the switching behavior of the GaN HEMT, but it also requires a more complex supporting circuit. Because the gate terminal directly drives the depletion-mode GaN HEMT, the gate drive circuit must provide voltage levels of about 0 V for turn-on and a negative voltage for turn-off (typically −12 to −14 V). The "enable" terminal is typically connected to the under-voltage lockout (UVLO) of the gate drive power supply so that the Si MOSFET is turned off when the gate drive circuit loses power. In contrast with the cascode variation, the Si MOSFET does not experience any switching during normal operation. When the low-voltage Si "enable switch" is off, the gate node of the GaN HEMT can no longer be shorted to its source node to turn on, thereby functioning as a normally off device.

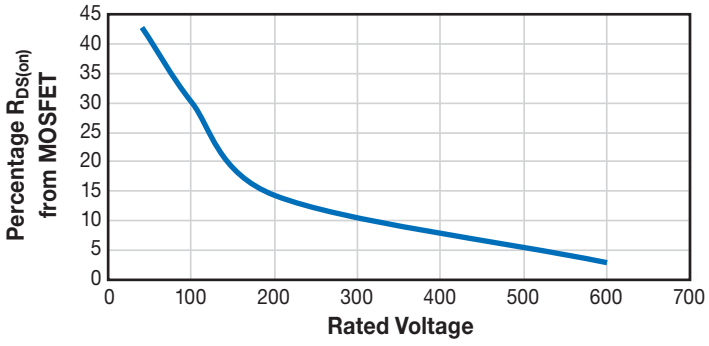

Figure 1.12 At a higher voltage rating the low-voltage MOSFET does not add significantly to the on-resistance of the cascode transistor system.

This type of solution for an enhancement-mode GaN "system" works well when the GaN transistor has a relatively high on-resistance compared with the low-voltage (usually 30 V rated) silicon MOSFET. Since on-resistance increases with the device breakdown voltage, hybrid solutions are most effective when the GaN transistor is high voltage and the MOSFET is very low voltage. In Figure 1.12 is a chart showing the added on-resistance to the cascode circuit by the enhancement-mode silicon MOSFET. A 600 V cascode device would only have about 3% added on-resistance due to the low-voltage MOSFET. Conversely, as the desired rated voltage goes down and the on-resistance of the GaN transistor decreases, the MOSFET contribution becomes more significant. For this reason, hybrid solutions are only practical at voltages higher than 200 V.

1.4.5 Reverse Conduction in HEMT Transistors

Enhancement-mode GaN transistors can also conduct in the reverse direction. When current is forced into the source of an "off" device, such as the case of a synchronous rectifier during its dead time, a voltage drop is created from source to drain. When the drain voltage becomes lower than the gate voltage by at least $V_{GS(th)}$ (see Figure 1.13b), the 2DEG is again restored under the gate electrode and current can flow from source

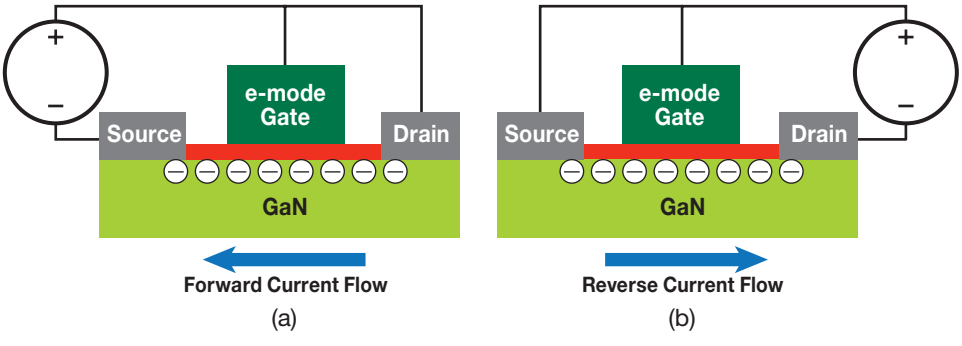

Figure 1.13 Enhancement-mode HEMT devices can conduct in either the forward or reverse direction.

to drain. Because the enhancement-mode HEMT has no minority carrier conduction, the device, operating similar to a diode, will turn off instantly when the forward bias is removed between the gate and drain electrodes. This characteristic is quite useful in certain power conversion circuits.

In the reverse direction, the cascode-connected transistor discussed in Section 1.4.4 conducts in the same way as an enhancement-mode GaN transistor, except that the diode of the MOSFET is conducting the reverse current, which then has to flow through the GaN device. The forward voltage drop of the MOSFET diode creates a slight positive voltage from gate to source in the HEMT which, therefore, is turned on in the forward direction. The HEMT on-resistance is added to the voltage drop of the MOSFET in this configuration. Unlike the enhancement-mode GaN transistor, the cascode-configured transistor does have a recovery time due to the injection of minority carriers in the silicon-based MOSFET.

1.5 Building a GaN Transistor

Building a GaN transistor starts with the process of growing the GaN/AlGaN heterostructure. There are four different starting bases, or substrates, that have been commonly used in fabricating GaN HEMT transistors: bulk GaN crystal, sapphire (Al_2O_3), SiC, and silicon.

1.5.1 Substrate Material Selection

The most obvious choice for a GaN device starting material would be a GaN crystal. The first attempts at growing GaN crystals were in the 1960s. Native defects from high nitrogen vacancy concentrations rendered these early attempts unusable for semiconductor device fabrication. Since then, progress has been made, and small-diameter, high-quality GaN crystals are becoming available, holding promise for use as a platform for active device fabrication.

Heteroepitaxy is a process whereby one type of crystal structure is grown on top of a different crystal. Because GaN crystals have not been readily available, much work has been focused on growing GaN crystals on top of a more convenient platform such as sapphire, SiC, or, more recently, silicon. The starting point for trying to grow on a dissimilar crystal layer is to find a substrate with the appropriate physical properties.

Referring to Table 1.2, it can be seen that there are tradeoffs between any of the three listed choices for a substrate material. For example, sapphire (Al_2O_3) has a 16.1% mismatch to a GaN crystal lattice and has poor thermal conductivity. Thermal conductivity is especially important in transistors for power conversion because they generate a significant amount of heat flux during operation due to internal power dissipation. SiC (6H–SiC) substrate, on the other hand, has a reasonably good lattice match and excellent thermal conductivity. The disadvantage comes from the cost of the starting crystal substrate, which can be up to 100 times the cost of a silicon substrate of the same diameter. Silicon is also not an ideal base for a GaN heteroepitaxial structure due to the lattice mismatch and the mismatch of thermal expansion coefficients. Silicon, however, is the least expensive material and there is a large and well-developed infrastructure to process devices on silicon substrates.

Table 1.2 Some key properties of Al_2O_3, SiC, and Si [18].

Substrate	Crystal Plane	Lattice Spacing Å	Lattice Mismatch %	Relative Thermal Expansion $10^{-5} \cdot K^{-1}$	Thermal Conductivity W/cm · K	Relative Cost
Al_2O_3	(0001)	4.758	16.1	-1.9	0.42	Middle
6H-SiC	(0001)	3.08	3.5	1.4	3.8	Highest
Si	(111)	3.84	-17	3	1.5	Lowest

For the reasons cited above, SiC is commonly used for devices that require very high-power densities, such as linear RF applications; silicon is used for devices in more cost-sensitive commercial applications such as DC–DC conversion, AC–DC conversion, class D audio amplifiers, and motion control.

1.5.2 Growing the Heteroepitaxy

There are several types of technologies that have been used to grow GaN on different substrates [19, 21–23]. The two most promising are metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). MOCVD is faster and generally lower in cost, whereas MBE is capable of more uniform layers with very abrupt transitions between layers. For GaN HEMT devices in power conversion applications, MOCVD is the dominant technology due to the cost advantages.

An MOCVD growth occurs in an inductively or radiantly heated reactor. A highly reactive precursor gas is introduced into the chamber where the gas is "cracked" by the hot substrate and reacts to form the desired compound. For GaN growth, the precursors are ammonia (NH_3) and trimethyl-gallium (TMG). For AlGaN growth, the precursors are trimethyl-aluminum (TMA) or triethyl-aluminum (TEA). In addition to the precursors, carrier gases such as H_2 and N_2 are used to enhance mixing and control the flow within the chamber. Temperatures in the range of 900–1100 °C are used for these growths.

A GaN heteroepitaxial structure involves at least four growth stages. Figure 1.14 illustrates this process. The starting material (a) of either SiC or Si is heated in the reaction chamber. A layer of AlN is then grown (b) to create a seed layer that is hospitable to the AlGaN wurtzite crystal structure. An AlGaN "buffer layer" (c) creates the transition to the GaN crystal (d). Finally, the thin AlGaN barrier is grown on top of the GaN crystal to create the strain layer that induces the 2DEG formation.

Earlier in this chapter, several methods of making enhancement-mode GaN transistors were described. One method (pGaN enhancement-mode), illustrated in Figure 1.10, includes an additional GaN layer grown on top of the AlGaN barrier. This layer is most commonly doped with p-type impurities such as Mg or Fe. A cross section of this heteroepitaxy structure is shown in Figure 1.15.

1.5.3 Processing the Wafer

Fabricating a HEMT transistor from a heteroepitaxial substrate can be accomplished in a variety of sequential steps. One example of a simplified process for making an enhancement-mode HEMT with a pGaN gate is shown in Figure 1.16. A cross section of a completed device using this process is shown in Figure 1.17.

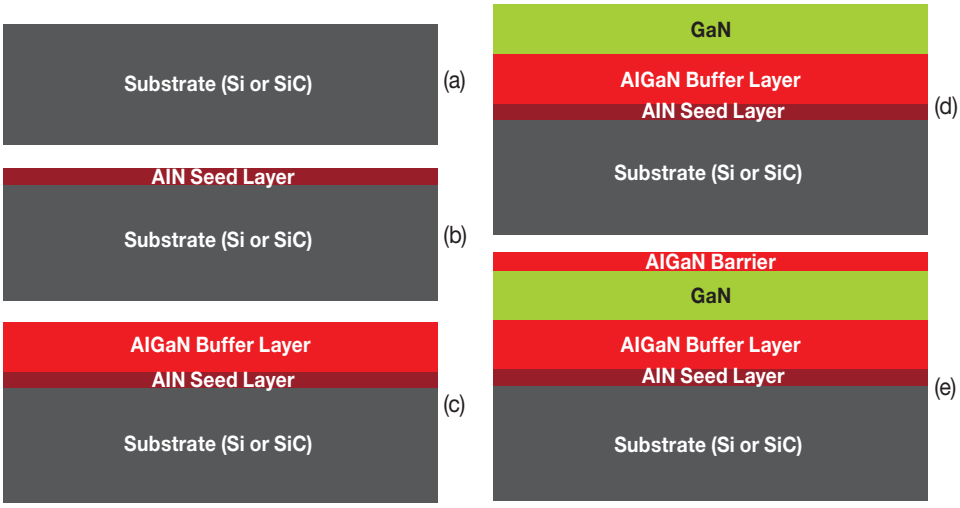

Figure 1.14 An illustration of the basic steps involved in creating a GaN heteroepitaxial structure (not to scale).

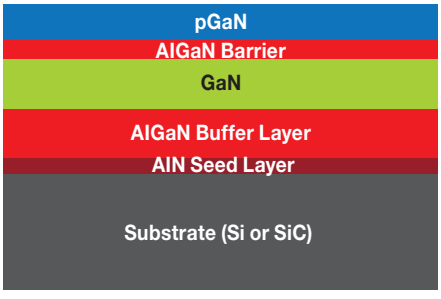

Figure 1.15 An additional GaN layer, doped with p-type impurities can be added to the heteroepitaxy process when producing an enhancement-mode device, as illustrated in Figure 1.10.

1.5.4 Making Electrical Connection to the Outside World

Following the device fabrication, provisions are needed to make the electrical connection to the electrodes of the device. There are two common ways of making connection to a power transistor: (i) attach bond wires between metal pads on the device and metal posts in a plastic or ceramic package or (ii) create contacts that can be soldered directly on the device while still in wafer form. As explored further in Chapter 3, GaN transistors are able to switch very quickly and, therefore, are very sensitive to inductances in either the power loop or the gate-source loop. Wire bonds have a significant amount of inductance and limit the ultimate capability of the GaN device. Wire bonding also increases the possibility for poor bonds, which can reduce the reliability of the final product [25–29]. It is for this reason that the preferred method for making an electrical connection is by soldering directly to contacts on the device. A common process for making these contacts that can be soldered is shown in Figure 1.18. The solder bars can either be a Pb–Sn composition or a lead-free composition of Ag–Cu–Sn.

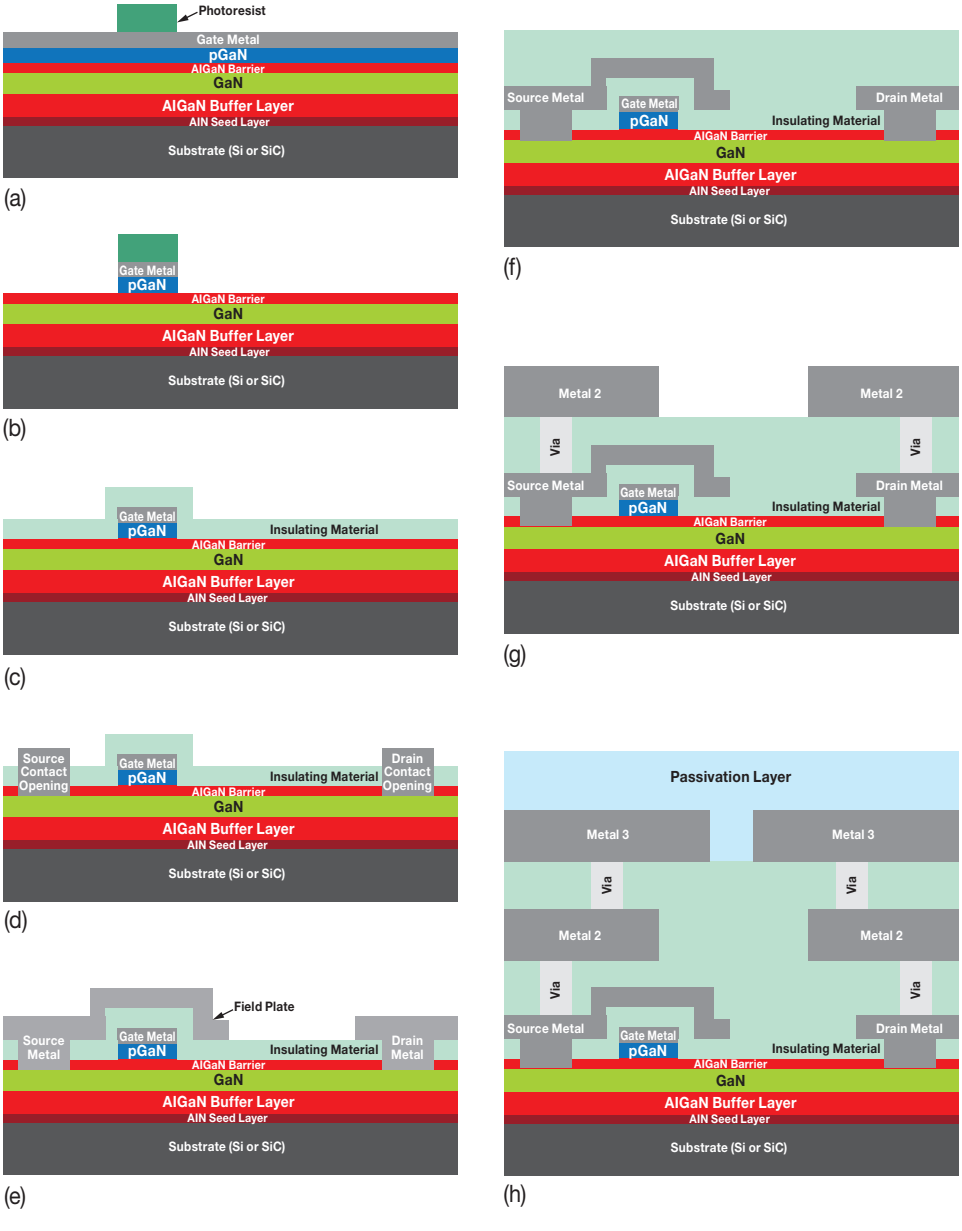

Figure 1.16 A typical process for fabricating an enhancement-mode GaN HEMT (not to scale) [24, 25]. The process steps are as follows: (a) Deposit gate metal and define gate pattern using photoresist as a protecting layer. (b) Etch the gate metal and pGaN crystal. (c) Deposit insulating material. (d) Create contact openings to source, drain, and gate (gate contact not pictured). (e) Deposit first aluminum metal layer and define metal pattern. (f) Deposit interlayer dielectric. (g) Cut vias between metal layers, form tungsten via plug, deposit and define second aluminum metal layer. (h) Deposit and define third aluminum layer and deposit final passivation layer.

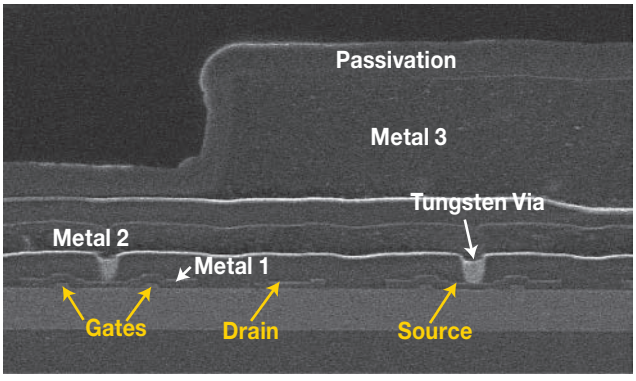

Figure 1.17 SEM micrograph of an enhancement-mode GaN HEMT made by Efficient Power Conversion Corporation [24–26].

Following solder bar formation, the completed wafer looks like the example in Figure 1.19. The individual devices are singulated and the final chip-scale transistor may look like the example in Figure 1.20. This device is now ready to be soldered on to a printed circuit board (PCB) or on to a lead frame to be incorporated into a plastic molded package.

1.6 GaN Integrated Circuits

Silicon-based power devices with rated voltages higher than about 20 V need to have vertical conduction paths due to the large separation required between source and drain terminals. Thanks to the higher critical electric field in GaN (see Section 1.3), GaN-on-Si devices can have a lateral conduction path while maintaining a very small size compared with Si-based MOSFETs. It is therefore straightforward to monolithically integrate multiple GaN-on-Si power transistors along with signal-level components. An early example of such single-chip integration is shown in Figure 1.21 [30].

This ability to integrate multiple functions monolithically holds the promise of producing a complete power conversion system on a single GaN-on-Si chip, a promise that, when realized, will significantly lower the cost and efficiency of power conversion.

The journey of integration has several steps, the first of which is to place multiple power devices on a single chip in a half-bridge configuration, as shown in Figure 1.22. This initial step is particularly compelling because a large percentage of power conversion applications revolve around this half-bridge topology. An early example of a monolithic half bridge is shown in Figure 1.23.

In Chapter 4 of this text, we will discuss the need for careful circuit layouts when using GaN devices. Circuit layouts need to have particularly low parasitic inductance. This is due to the extremely fast switching speed that, when combined with small amounts of inductance, and by virtue of the relationship between inductance (L), voltage (V), and fast changes in current ($\mathrm{d}i/\mathrm{d}t$) shown below, switching losses can be increased and large, unwanted voltage spikes can be generated:

$$V = L \cdot \mathrm{d}i / \mathrm{d}t \tag{1.5}$$

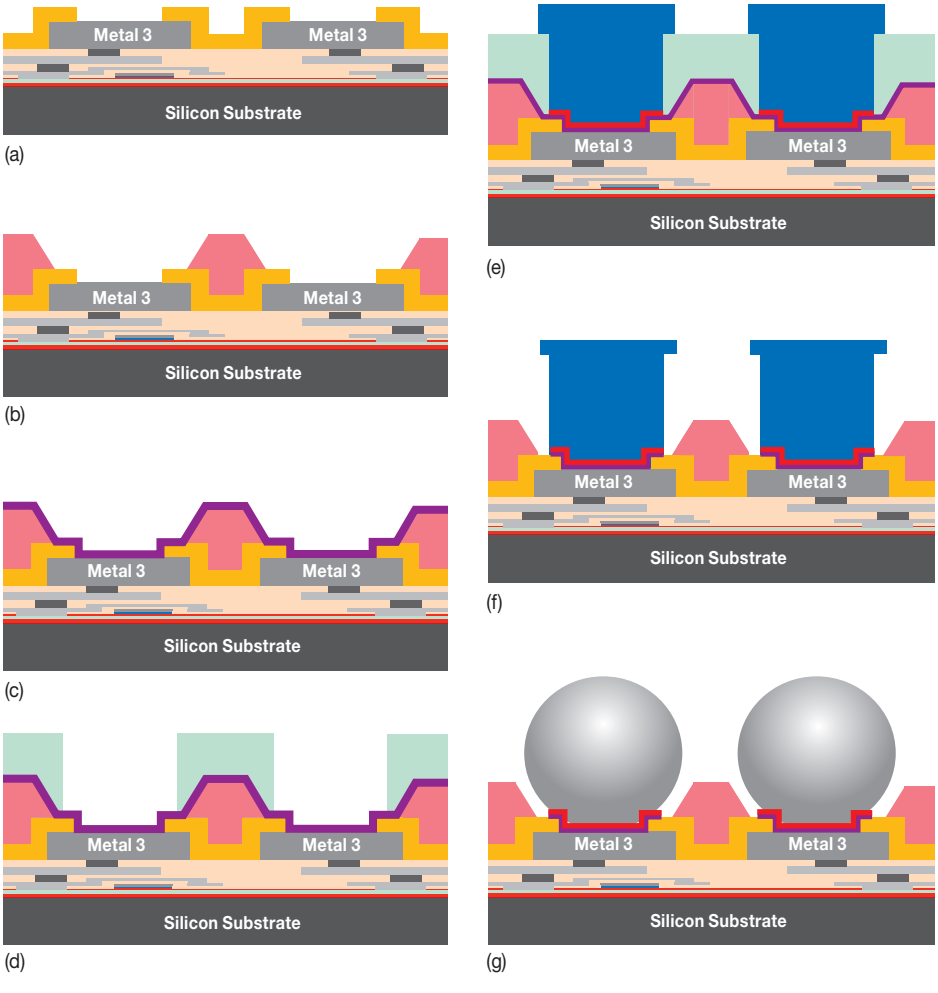

Figure 1.18 A typical process for creating solder bars on an enhancement-mode GaN HEMT (not to scale). The basic process steps are as follows. (a) The finished wafer with openings in the passivation. Metal layer 3 is partially exposed. (b) Photopolyimide is deposited and removed in the area where the solder is desired. (c) An under-bump metal is deposited to create an interface between the aluminum top metal and the solderable material. (d) Photoresist is used to define where the solder will be plated. (e) Copper and solder are plated in the opening. (f) The photoresist is removed, and the under-bump metal is etched. (g) The solderable metal is reflowed to form elongated solder bars.

A monolithic half bridge has several advantages; a small transistor with a large aspect ratio can reside next to a large transistor, the overall system area is reduced by eliminating the need for space on the PCB allocated to two discrete devices, and the parasitic inductance coming from the copper between discrete devices on the PCB is eliminated. This latter advantage can be seen more clearly in Figure 1.24. At higher output currents in a simple buck converter (see Chapter 7), the parasitic power loop inductance becomes a key contributor to power losses. In Figure 1.24 a 12–1 V buck converter with two monolithic half bridges in parallel has an efficiency at 1 MHz and 40 A of about 87.5%, compared with about 85% for discrete devices of approximately the same size and on-resistance.

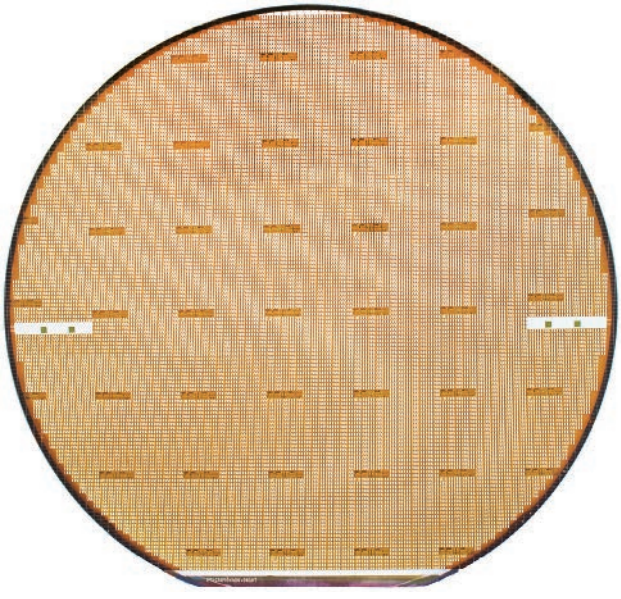

Figure 1.19 A completed 150 mm diameter enhancement-mode GaN HEMT wafer with approximately 20 000 individual power transistors.

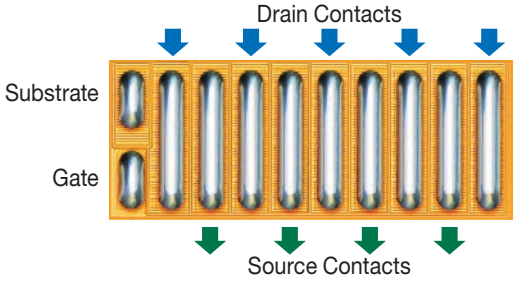

Figure 1.20 A finished chip-scale device with solder bars in Land Grid Array (LGA). This device measures approximately 4 mm × 1.6 mm.

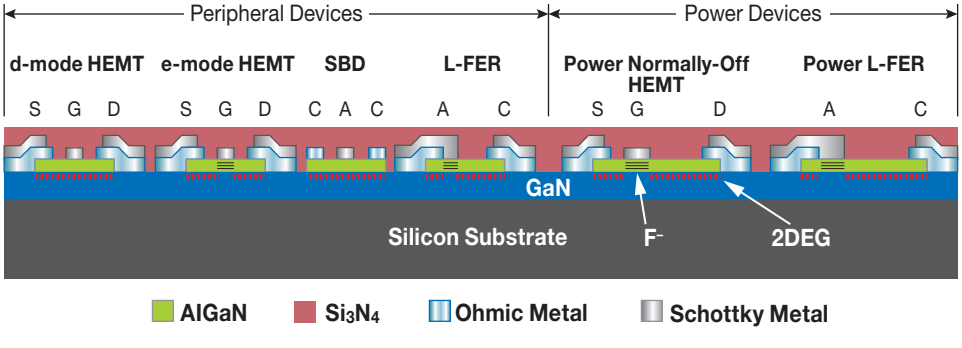

Figure 1.21 An early example of a GaN-on-Si integrated circuit including multiple power devices and signal level devices on the same chip [30]. (*Source:* Image is by courtesy of Kevin Chen, Hong Kong University of Science and Technology.)

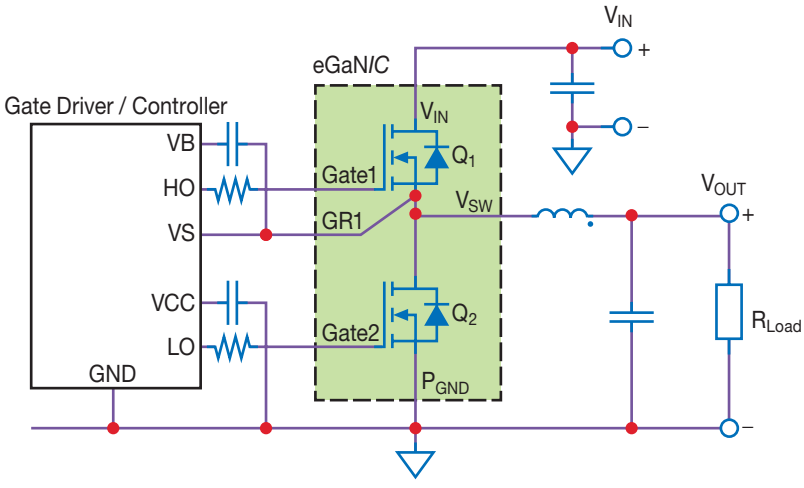

Figure 1.22 The half-bridge circuit is one of the most common circuit topologies used in power conversion. Shown here is a half bridge in a buck converter. The components inside the dotted lines (eGaN®IC) can be integrated monolithically.

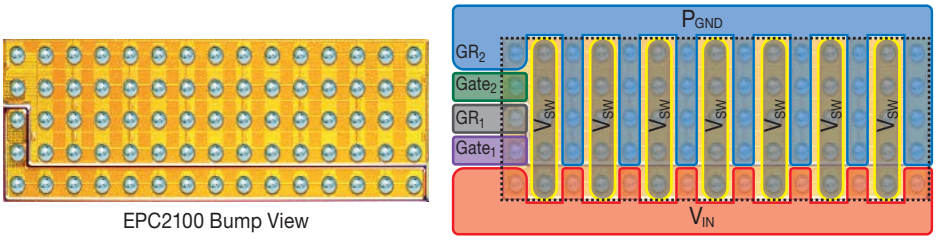

Figure 1.23 The first monolithic enhancement-mode GaN-on-Si half-bridge IC was the EPC2100 launched in 2014. This device measures 6 mm × 2.3 mm and has a BV_{DSS} = 30 V on both high-side and low-side transistors [31]. On the left is a photo of the die and on the right are the pin assignments as per Figure 1.22.

Following the production of a monolithic half bridge, the next logical step on the path to a GaN-on-Si power system on a chip is to add a driver to the power transistor. This driver can provide the interface to a logic device, such as a microcontroller, and can eliminate some of the sensitive design and layout requirements that are discussed in Chapters 3 and 4. Figure 1.25 shows a block diagram of the driver circuit that is most commonly needed in a GaN-based power conversion system, while Figure 1.26 is the chip-scale integrated circuit in a ball grid array (BGA) format that implements the functions inside the dotted line in Figure 1.25.

As discussed in Chapters 3 through 17 of this book, most power conversion applications have at their core a half bridge in some form. This half bridge requires drivers and a level shifting function to drive and synchronize the high-side transistor. A basic block diagram of the half bridge with drivers and level shifting is shown in Figure 1.27, while Figure 1.28 is the chip-scale integrated circuit in a BGA format that implements the functions shown in Figure 1.27.

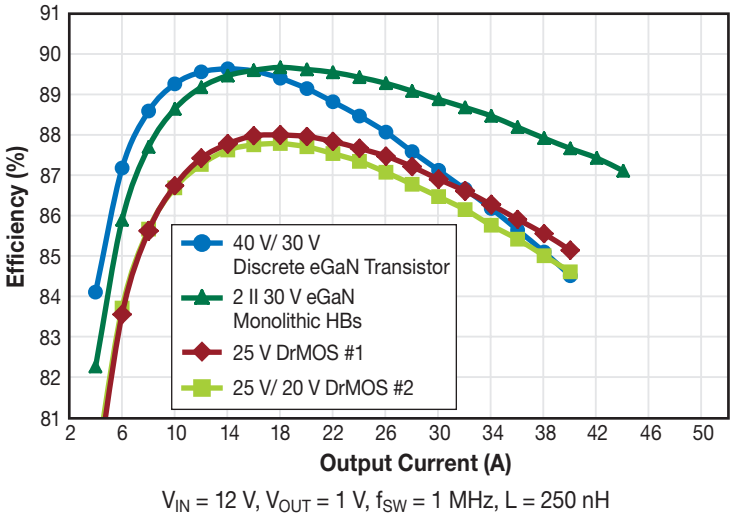

Figure 1.24 Total buck converter efficiency with the EPC2100 half bridge compared with discrete GaN transistors and discrete MOSFETs [32].

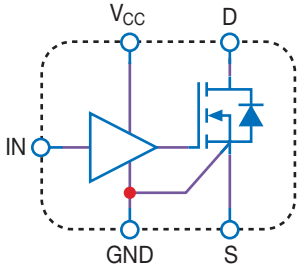

Figure 1.25 Block diagram of the driver circuit and the power transistor most commonly required in a power conversion system.

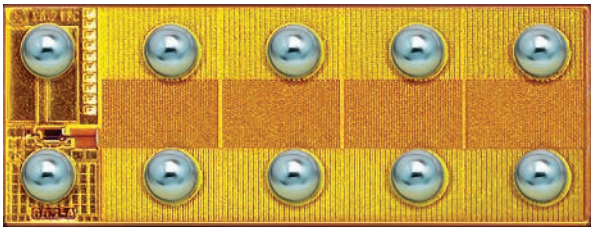

Figure 1.26 The EPC2112 integrated circuit [33] introduced in March 2018 has a driver integrated monolithically with the 200 V, 40 mΩ enhancement-mode transistor. This chip-scale device in a BGA format measures 2.9 mm × 1.1 mm.

Once the building block of a half bridge with drivers and level shift has been developed, the door is open for producing a wide variety of integrated circuit variants, such as full-bridge converters and three-phase power stages. In addition, it is straightforward to add functions and features such as analog or digital interfaces and controls.

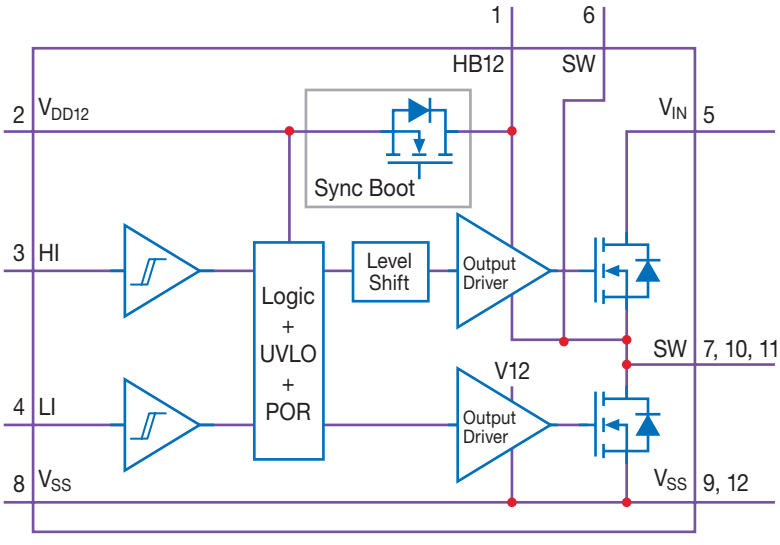

Figure 1.27 Block diagram of the driver circuits, level shift, and the power transistors most commonly required in a power conversion system.

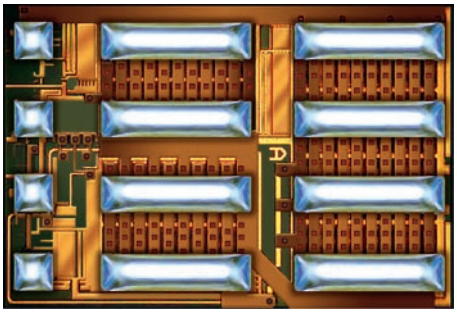

Figure 1.28 The EPC2151 integrated circuit has drivers and level shifting integrated in a single chip with the two 100 V enhancement-mode transistors in a half-bridge configuration. This device measures 3.9 mm × 2.6 mm and conducts 10 A at 1 MHz with 48 V_{IN} and 12 V_{OUT}.

One limitation to even greater integration of functions, however, is that the technical challenge of creating a complimentary p-channel transistor to work with the enhancement-mode HEMT has yet to be met. As discussed in Section 1.2, GaN is a great host for a HEMT due to the ability to create a 2DEG. There have been numerous works demonstrating a two-dimensional hole gas (2DHG) [34], but overall hole mobility, typically less than 20 $cm^2/V \cdot s$ is too poor to make a competitive complementary MOS (CMOS) circuit. Many other alternatives, including creating silicon-based p-channel devices in the silicon substrate, either beneath or beside a GaN epitaxial layer, have also been explored but no commercial devices have been realized as of the date of this publication.

1.7 Summary

In this chapter, a new platform for making switching power transistors using GaN grown on top of a silicon substrate was introduced. Enhancement-mode transistors have in-circuit characteristics very similar to power MOSFETs, but with improved switching speed, lower on-resistance, and at a smaller size than their silicon predecessors. These new capabilities, married with a step forward in chip-scale, high-density packaging, enable power conversion designers to reduce power losses, reduce system size, improve efficiency, and, ultimately, reduce system costs.

Chapter 2 will connect these basic physical properties of GaN transistors to the electrical characteristics most important in designing power conversion systems. These electrical characteristics will be compared to state-of-the-art silicon MOSFETs in order to illustrate both the strong similarities and the subtle differences. In Chapters 3 through 16, these same electrical characteristics will be related to circuit and system performance in such a way as to give the designer the tools to get the maximum performance from GaN devices.

Finally, in Chapter 17, the "why, when, and how" that GaN transistors will displace MOSFETs is discussed. Included is a discussion of cost trajectories, reliability, and technology directions for the years 2014 through 2020.

These are the early years of a great new technology.

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